

# CLAIMS

- 1 1. A flash memory device formed from a substrate, the device comprising:  
2 strings of transistors of a NAND architecture comprising a first select gate, a  
3 plurality of floating gates, and a second select gate,  
4 each floating gate having at least two sides perpendicular to the axes of the  
5 strings;  
6 a conductive isolating member adjacent to each of the at least two perpendicular  
7 sides of the floating gate and located between adjacent transistors in the strings of  
8 transistors, each isolating member shielding a selected floating gate from a charge stored  
9 in an adjacent component.
- 1 2. The flash memory device of claim 1, wherein the floating gates are formed  
2 between shallow trench isolation areas and wherein the device further comprises  
3 wordlines extending across adjacent strings and extending between the floating gates into  
4 the shallow trench isolation areas thereby isolating adjacent floating gates.
- 1 3. The flash memory device of claim 1 wherein the isolating members have two  
2 principal faces, the faces substantially parallel to the at least two sides of each floating  
3 gate and substantially perpendicular to the axes of the strings.
- 1 4. The flash memory device of claim 1 wherein the isolating members extend a  
2 distance between the substrate and an upper level of the floating gates.
- 1 5. The flash memory device of claim 4 wherein the floating gates have an upper  
2 level and a lower level, the isolating members extending from the substrate a distance  
3 between the lower and upper level.
- 1 6. The flash memory device of claim 1, wherein the isolating members and the  
2 wordlines comprise a conductive material, and wherein the isolating members are  
3 electrically connected to a wordline above a floating gate that the isolating members  
4 shield.
- 1 7. The flash memory device of claim 6 wherein the floating gates are approximately  
2 T shaped, and wherein isolating members electrically coupled to the wordlines flank the  
3 floating gates.

1     8.     The flash memory device of claim 1 wherein the isolating members shield a  
2 floating gate of the plurality of floating gates from an electrical field of an adjacent  
3 floating gate, thereby minimizing field effect coupling between adjacent floating gates.

1     9.     The flash memory device of claim 8 wherein the adjacent floating gate is  
2 diagonally adjacent or horizontally adjacent to the selected floating gate and wherein the  
3 isolating members further minimize field effect coupling in the wordline direction.

1     10.    A non-volatile memory device comprising:  
2 floating gates that store a charge;  
3 bitlines that select amongst the floating gates, each bitline having a bitline axis;  
4 wordlines that select amongst the floating gates; and  
5 sidewall elements positioned along the bitline axes, the sidewall elements located  
6 at sides of the floating gates between adjacent floating gates, the sidewall elements  
7 shielding the floating gates.

1     11.    The memory device of claim 10 wherein the sidewall elements shield the floating  
2 gates from an electrical field having a component in the direction of the bitline axes.

1     12.    The memory device of claim 10 wherein the sidewall elements extend from the  
2 substrate to the floating gates.

1     13.    The memory device of claim 12 wherein the floating gates have an uppermost  
2 and a lowermost surface, the sidewall elements extending from the substrate until or  
3 beyond the level of the lowermost surface.

1     14.    The memory device of claim 12 wherein the floating gates have an uppermost  
2 and a lowermost surface, the sidewall elements extending from the substrate until or  
3 beyond the level of the uppermost surface.

1     15.    The memory device of claim 10 wherein the sidewall elements comprise a  
2 conductive material and wherein the sidewall elements are electrically coupled to a  
3 wordline located between adjacent pairs of sidewall elements.

1     16.    The memory device of claim 15 wherein the coupled sidewalls effectively  
2 increase the surface area of the wordline and the electrical coupling between the wordline  
3 and the floating gates, thereby aiding in read and write operations.

1 17. The memory device of claim 10 wherein the wordlines extend between adjacent  
2 floating gates so as to shield a selected floating gate from an electrical field of adjacent  
3 floating gates, and wherein the non-volatile storage device is NAND flash memory.

1 18. A method of forming NAND flash memory comprising:  
2 forming floating gates;  
3 forming control gates above the floating gates;  
4 forming bitlines, the bitlines used together with the control gates to read and write  
5 from a floating gate,  
6 the direction of the bitlines substantially perpendicular to the direction of the  
7 control gates, the floating gates having bitline sides in the bitline direction and control  
8 gate sides in the control gate direction;  
9 forming members on the bitline sides of the floating gates, the members shielding  
10 the floating gates from electrical fields having a component in the bitline direction.

1 19. A flash memory device comprising:  
2 floating gates for storing data located above a substrate;  
3 means for isolating adjacent floating gates in the wordline direction;  
4 means for isolating adjacent floating gates in the bitline direction; and  
5 means for reading the data stored in the floating gates, the means for reading the  
6 data located above the floating gates and interconnecting strings of floating gates, the  
7 means for isolating adjacent floating gates in the bitline direction electrically connected to  
8 the means for reading the data.

1 20. The flash memory device of claim 19 wherein the means for reading the floating  
2 gates extends within the means within the substrate for isolating adjacent floating gates.

1 21. The flash memory device of claim 20 wherein the means for reading shields  
2 adjacent floating gates from Yupin effect errors and from disturbs.

1 22. A method of making a memory device in a substrate comprising:  
2 forming a series of floating gates between a first set of trenches each floating gate  
3 having two approximately parallel bitline sides and two approximately parallel roughly  
4 rectangular wordline sides;  
5 forming a second set of parallel trenches in an oxide layer deposited within the  
6 first set of trenches;

7           forming a wordline above adjacent floating gates, the wordline extending into the  
8   second set of trenches and isolating one of the floating gates from a charge applied at an  
9   adjacent floating gate; and

10          forming a conductive element at each of the approximately parallel bitline sides of  
11   the floating gates.

1   23.    The method of claim 22 wherein the conductive elements are located on both  
2   sides of a floating gate and wherein the method further comprises electrically contacting  
3   the elements to the wordline that selects the floating gate.

1   24.    The method of claim 23 wherein the conductive elements shield a selected  
2   floating gate from an electrical field of an adjacent floating gate and minimize field effect  
3   coupling in the bitline direction between adjacent floating gates.

1   25.    The method of claim 24 wherein the adjacent floating gate is diagonally adjacent  
2   or horizontally adjacent to the selected floating gate and wherein the conductive elements  
3   further minimize field effect coupling in the wordline direction.

1   26.    The method of claim 22 wherein the memory device formed is a NAND flash  
2   memory device.